Remarks

Claims 1-14 are currently pending in the patent application. Claim 1 is presently amended to correct a clerical error, and new claims 15-19 are presented added. Applicant submits that the amendments are fully supported by the specification as originally filed, and that no new matter has been added. For the reasons and arguments set forth below, Applicant respectfully submits that the claimed invention is allowable over the cited references.

In the non-final Office Action dated March 26, 2008, the following rejection is indicated: claims 1-14 stand rejected under 35 U.S.C. § 102(b) over the Melanson reference (U.S. Patent No. 6,294,954). Applicant traverses this rejection.

The § 102(b) rejection of claims 1-14 is improper because the Melanson reference fails to teach all of the features recited in Applicant's claims. In particular, Melanson fails to disclose measuring and correcting for differences between an on-delay of input and output signals and an off-delay of input and output signals, for example to reduce distortion in a digital amplifier. Instead, Melanson is directed to reducing the dead time between switching of two switches without creating overlap. Melanson's circuit does not involve measuring differences between input and output signals, and in particular does not involve detecting pulse edge delays between the rising and falling edges of input and output signals to determine an on/off difference as recited in Applicant's claims. As indicated in Figs. 5a and 5b, Melanson's circuit uses a single measurement to determine the degree of dead time or overlap between switching for a given pair of switches. Such measurement could not be used to develop an error signal based on Applicant's recited on/off difference, which represents the difference between on-delays of an input and output signal and off-delays of the input and output signal. Applicant finds nothing in Melanson to teach or suggest measuring on-delays or off-delays between input and output signals, much less correcting for a difference between them.

For at least these reasons, the Melanson reference cannot be properly read to teach all of the features recited in Applicant's claims. Applicant therefore submits that the § 102(b) rejection is improper, and requests that it be reconsidered and withdrawn.

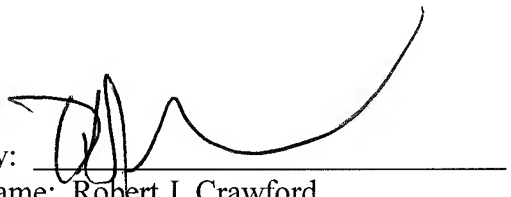
Applicant further submits that the art of record does not appear to teach or suggest the subject matter additionally recited in newly added claims 15-19. In particular, the

applied art does not disclose a pulse edge delay detector having a subtractor that determines the on/off-difference from measured on-delays and off-delays, or an error signal generator having an integrator (such as an integration capacitor) that integrates the on/off-difference to produce the error signal, as recited in claims 15-17. Moreover, the applied art does not disclose an input pulse delay circuit that controls charging and discharging of the gate capacities of MOSFET switches, for example based on switching current sources one of which is controlled by the error signal, as recited in claims 18 and 19.

In view of the remarks above, Applicant believes that each of the rejections/objections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063.

Please direct all correspondence to:

Corporate Patent Counsel
NXP Intellectual Property & Standards
1109 McKay Drive; Mail Stop SJ41
San Jose, CA 95131
CUSTOMER NO. 65913

By: 
Name: Robert J. Crawford
Reg. No.: 32,122
(NXPS.522PA)